THD COMPARISON OF DISTINCT LEVELS OF CASCADED H-BRIDGE CONVERTERS WITH A NOVEL SPWM TECHNIQUE

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Abstract – Cascaded H-Bridge multilevel converters are popular for their robust design structure and transformer less operation. The paper presents a novel SPWM control technique called Sinusoidal Pulse Width Modulation-Variable Modulation Index strategy (SPWM-VMI) applied on four different levels (5, 7 and 9) of cascaded H-Bridge multilevel converters. This technique is adopted to reduce the total harmonic distortion in lower levels of the converter so as to alleviate the hardware requirement. The modulation index is varied in each H-Bridge cell following a hyperbolic arrangement. This results in much lower THD in low level converters than conventional SPWM techniques.

Keywords – Cascaded H-Bridge Multilevel converters, five level converter, seven level converter, nine level converter, modulation index (MI), Total Harmonic Distortion (THD).

I. INTRODUCTION

Multilevel converters are becoming popular due to their modular design structure and simplicity in operation [1]. Cascaded H-Bridge topology with advanced control strategies has become a prominent topic of research among scholars for various applications. The multilevel converter can generate different levels of output voltage which can be compared with a staircase arrangement [1][2][3]. Power semiconductor switches are arranged in different patterns implying to generate multilevel output of voltage waveform. These patterns constitute topologies like diode clamped, capacitor clamped, cascaded H-Bridge structure and upcoming asymmetric multilevel converters. Topologies like diode clamped and flying capacitor are now being overcome by cascaded H-Bridge structures and asymmetric converters as it does not utilize freewheeling diodes or clamping capacitors [2].

The power semiconductor switches employed in these converter designs are triggered by control methodology which is compatible with the design topology. The most popular methods of firing the switches are selective harmonic elimination (SHE), space vector control (SVC) and Sinusoidal pulse width
modulation (SPWM). SHE shows excellent results for diode clamped converter while it depicts to be fair scheme for capacitor clamped but SPWM control technique is proved out to be the best methodology for cascaded H-Bridge structure [5]. This is more precisely explained in Fig.1.

![Control Techniques of Multilevel Converters](image)

**Fig.1 Control techniques of multilevel converters.**

**A. Cascaded H-Bridge Design Structure**

Four semiconductor switches are connected in a particular arrangement (in alphabet ‘H’ pattern) supplied by a fixed dc source is called as single H-Bridge cell such that it produces a three level output of voltage waveform. Alike H-Bridge cells are connected in series connection to obtain multiple levels of output waveform. As the number of bridges is increased, the number of levels is also increased and the generated multilevel output is in close agreement with the sinusoidal output [2][3].

The total harmonic distortion is the measure of distortion in the waveform calculated by Eq. 1 [4].

$$\text{THD} = \sqrt{\frac{\sum_{n=2}^{\infty} (V_n)^2}{V_{01}}}$$  \hspace{1cm} (1)

The ratio of RMS values of output voltage comprising all the harmonic components to the fundamental component of output voltage gives the THD of output voltage. The fundamental component of output voltage is obtained from Eq.2 [6].

$$V_{01} = 4bV_s/\pi \sqrt{2}$$  \hspace{1cm} (2)

The accustomed design structure of cascaded H-Bridge multilevel converter is depicted in Fig.2.

![Cascaded H-Bridge Topology](image)

**Fig.2 Cascaded H-Bridge topology**

**Sinusoidal Pulse Width Modulation**

N number of carrier pulses is required to generate N+1 levels of output voltage. The reference voltage signal is kept constant whereas the amplitude of carrier signals in each H-Bridge cell is changed so as to obtain variable Modulation Index ‘m’.

The modulation index is defined as the ratio of the amplitude of reference signal to that of the carrier signal. The value of modulation index determines the width of the control pulse. Lower the carrier pulse amplitude higher will be the modulation index value and vice versa.

**II. MODELLING AND SIMULATION**

Three distinct models viz. five, seven and nine levels of cascaded H-Bridge Multilevel converters are designed for 400V DC to AC conversion with a new SPWM control paradigm. In this each of the H-Bridges are controlled by a pulse width modulated pulses but with a different modulation index value (MI) for carrier pulses. The MI value which is the ratio...
of the magnitude of reference sinusoidal pulse to the carrier pulse is varied by varying the amplitude of triangular carrier pulse signal in every H-Bridge cell of the converter. Table 1 depicts the obtained MI values for the converters.

### Table 1 Modulation Index (MI) values for the converters

<table>
<thead>
<tr>
<th>S.No</th>
<th>No. of Levels</th>
<th>No. 1</th>
<th>No. 2</th>
<th>No. 3</th>
<th>No. 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Five</td>
<td>1</td>
<td>0.94</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>2</td>
<td>Seven</td>
<td>1</td>
<td>0.85</td>
<td>1</td>
<td>-</td>
</tr>
<tr>
<td>3</td>
<td>Nine</td>
<td>1</td>
<td>0.92</td>
<td>0.92</td>
<td>1</td>
</tr>
</tbody>
</table>

The multilevel converters designed by using the different MI values for each bridge is employed to convert 400V DC to corresponding staircase pattern of AC voltage with five, seven and nine levels as shown in Fig. 4 (a), (b) and (c). Series R-L load consuming 2000W of active power 1000W of reactive power is connected across the output terminals of every converter. The simulated results generated on the basis of total harmonic distortion of output voltage are depicted in Fig. 5.

A significant comparison is observed in terms of THD by utilizing a low pass filter to eliminate the higher order harmonics of the output voltage waveform.

### III. RESULT AND DISCUSSION

Fig. 3 SPWM sequences of control pulse for multilevel converters (a) five level (b) seven level and (c) nine level.

If carrier pulses are compared with the reference signal, the SPWM sequences of control pulse described in Fig.3 (a), (b) and (c) are obtained to trigger the switches of five, seven and nine level converter respectively.

Fig. 4 Stepped voltage output of (a) five level (b) seven level and (c) nine level converter.
Table 2 Comparative Analysis of Multilevel Modulation Techniques

<table>
<thead>
<tr>
<th>S. No.</th>
<th>No. of levels</th>
<th>SPWM</th>
<th>APWM</th>
<th>Basic Volt</th>
<th>Load Current</th>
<th>Calculated</th>
<th>Standard</th>
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<tbody>
<tr>
<td>1</td>
<td>Five</td>
<td>24.34</td>
<td>22.30</td>
<td>1.63</td>
<td>2.08</td>
<td>360.12</td>
<td>359.8</td>
</tr>
<tr>
<td>2</td>
<td>Seven</td>
<td>24.26</td>
<td>20.30</td>
<td>1.27</td>
<td>1.98</td>
<td>360.12</td>
<td>359</td>
</tr>
<tr>
<td>3</td>
<td>Nine</td>
<td>17.39</td>
<td>21.41</td>
<td>1.20</td>
<td>1.12</td>
<td>360.12</td>
<td>360.3</td>
</tr>
</tbody>
</table>

IV. CONCLUSION

A novel SPWM control technique by varying the modulation index in each H-Bridge cell has been developed and applied on different levels of cascaded H-Bridge multilevel converter models in this paper. This technique is suitable for lower levels of multilevel converters such as five level and seven level as a reduction in percentage THD is achieved than the THD generated by applying conventional SPWM control strategy. This control is relevant with the existing systems because by only changing the MI value and without replacing the structural topology the THD can be alleviated thereby the cost of replacement of multilevel converter can be avoided.

References


