SIMULATION OF NANOSCALE TFET DEVICE STRUCTURE FOR LOW POWER APPLICATION

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Abstract—The scaling has been a main key for continuous progress in silicon-based semiconductor industry over the past four decades. However, as the technology advancement in nanometer scale regime for the purpose of building ultra-high density integrated electronic computers and extending performance, CMOS devices are facing many serious problems such as increased leakage currents, difficulty on increase of ON-current, large process parameter variations, short channel effects, low reliability and yield, increase in manufacturing cost, etc. Tunnel FETs are interesting devices for ultra-low power applications due to their steep sub-threshold swing (SS) and very low OFF-current.

Keywords- CMOS, nanoscale, high-density, leakage current, ON-current, OFF-current, SS, BTBT, TFET.

I. INTRODUCTION

In nanoscale regime ultra low power consumption is a key challenge for the integrated circuit design. In recent years, there are many novel nanoscale semiconductor devices such as DG MOSFET, FinFET, Gate-All Around (GAA), Tunnel FET etc. studied to obtain a minimum $I_{OFF}$ and a maximum ratio of $I_{ON}/I_{OFF}$ as well as high ON current to avoid these limitations. The Tunnel FETs are considered as alternating switching devices for low power applications to mitigate the problems of conventional MOSFETs. This limits the ON current ($I_{ON}$) and the $I_{ON}/I_{OFF}$ ratio severely as the supply voltage is reduced. Many researchers have shown interest in TFET for its better Sub-threshold Swing (SS) which avoids the limit of 60 mV/decade at room temperature in MOSFETs, and provides low OFF-state current ($I_{OFF}$) and better SCEs due to inter-band tunneling current transport mechanism for the structure of gated reverse biased p-i-n transistor [1-5]. Since, TFETs offer the potential for a low off current and a small SS, but they generally have a lower on current than conventional MOSFETs, so a smart design strategy could achieve a small SS average and a high ION without degrading $I_{OFF}$. So that, major technology boosters for all-silicon TFETs include [2, 6] the use of a high-$\kappa$ gate dielectric.

II. REVIEW OF TFET

Tunnel transistors which use BTBT to inject carriers into the channel instead of injecting carriers over a barrier are not limited by 60 mV/decade turn-off [7]. These tunneling transistors (TFETs) are therefore of great interest for high $I_{ON}/I_{OFF}$ at low voltages. TFET performance is limited by the BTBT generation rate which is exponentially dependent on the effective tunneling bandgap as well as effective carrier mass of the semiconductor [8]. The obvious means to enhance TFET performance and scale $V_{DD}$ is by scaling this effective tunneling bandgap. This can be achieved by moving from Si to Ge to even lower bandgap III-V materials [9]. Since low $I_{OFF}$ keeps the standby power consumption low, a TFET with lowest $I_{OFF}$ and largest $I_{ON}/I_{OFF}$ at a reduced $V_{DD}$ is desired for ultra-low voltage operation. Among the most studied and optimized TFETs architectures, thin film Double-Gated (DG) lateral p-i-n TFET [2, 10] and a p-i-n TFET with a delta-doped n+ at the source side are shown to offer remarkable for obtained high $I_{ON}/I_{OFF}$ ratio and good output characteristics. TFETs retain their excellent switching characteristics even at high temperature because the tunneling mechanism makes them almost insensitive to temperature changes. TFETs offer a solution for critical leakage power savings in Static Random Access Memory (SRAM). Six-transistor (6T) [11] and 4T [12] SRAM cell designs with CMOS and TFET technologies have been compared in terms of layout, performance and power on silicon platforms. A 700-fold improvement in leakage reduction over CMOS technology with a voltage supply of 0.3V was demonstrated in the silicon TFET SRAM. Other attractive applications of TFETs are in analog integrated circuits such as ultralow-power voltage-controlled oscillators and voltage references that have to deliver a well-defined...
output voltage, independently of supply voltage, temperature and process variations.

III. TFET PRINCIPLE OF OPERATION.

The origins of the nanoscale semiconductor device i.e. TFET and Impact-Ionization Metal–Oxide–Semiconductor (IMOS) transistors [13] have been analyzed as candidates for future small slope electronic switches. It has been demonstrated that can offer significant power savings, especially in the standby mode. These new categories of switches have applications for ultra-low power logic and/or as power gating devices for future power management. The operating principles of the TFET can be easily understood with the help of the energy band diagram and device cross section as shown in figure 1. It shows that channel current flows by Zener tunneling mechanism [14] from valance band to conductance band. A gate is aligned to the p+ n+ in such a way so that the p+ n+ junction and a metal work function selected to fully deplete the channel configured for normally OFF state. According to figure 1 by the Zener tunneling mechanism the transistor turn ON with a saturated current. This saturated current is set by the gate to source voltage. The transistor is fully depleted without gate bias. In turning the transistor ON, the gate bias lowers the vertical electric field normal to the gate, opposite to the case of the MOSFET where the effective mobility degrades with increasing vertical field. This embodiment of the TFET can be expected to have lower Coulomb scattering than a MOSFET or a p-i-n TFET.

The physics of Band-to-Band Tunneling (BTBT) phenomena is based on Wentzel-Kramers-Brillouin (WKB) approximation. The BTBT modes (lateral and vertical tunneling) that can be employed in a TFET. The vertical tunneling in the direction perpendicular to the semiconductor/gate-dielectric interface offers multiple advantages which make it attractive over the original TFET design. One challenge in TFETs is to realize high ON currents because $I_{on}$ critically depends on the transmission probability, $T_{WKB}$, of the inter-band tunneling barrier. This barrier can be approximated by a triangular potential, as indicated by the grey shading in fig. 2b, so $T_{WKB}$ can be calculated using the WKB approximation [1]. Where $m^*$ is the effective mass and $E_g$ is the bandgap. Here, $\lambda$ is the screening tunneling length and describes the spatial extent of the transition region at the source–channel interface shows in figure 2; it depends on the specific device geometry.

IV. STRUCTURE OF TFET

The Tunnel FET is a gated reverse biased p-i-n based diode structure along with the channel which can be used as a transistor by using a gate contact to control the band bending in the channel region based on the interband tunneling effect which shown in figure 3. The only structural difference associated with a TFET is in the asymmetrically doped source and drain regions (p+i-n+) in TFET vs. symmetrically doped source and drain regions (n+p-n+) of a MOSFET [15]. The operation of a
MOSFET is based on Gate-Voltage ($V_{G}$) modulation of the channel potential for the injection of carriers over the barrier height from the source into the channel region through a process called thermionic emission.

The operation of a TFET also relies on gate-voltage modulation of the channel potential for the injection of carriers (electrons for an n-channel and holes for a p-channel MOSFET) from the source into the channel region. However, in contrast to an injection over the potential barrier (i.e. thermionic emission) in a MOSFET, the carriers are injected into the channel through the potential barrier via a process called Band-To-Band Tunneling (BTBT) [16]. Although a detailed discussion on the tunneling phenomena will be presented in the main advantage associated with BTBT is that the energy band gap (of magnitude $E_{g}$) cuts off the Boltzmann “tail” of the electrons in the p-type source region (holes for the n-type source region). This lack of thermal (‘$kT$’) dependence permits sharper than 60 mV/decade turn-on characteristics at room temperature, when the conduction band of the channel overlaps with the valence band of the source region. The resulting tunneling current can be expressed as in eq. 2 [16]

$$I_{BTBT} \approx Ae^{2}\exp \left[ -\frac{B}{E_{g}} \right]$$  \( (2) \)

Where A and B are material dependent parameters. When a TFET is in the OFF-state, the p-i-n structure of a TFET is reverse-biased and hence the diode leakage current comprises the dominant source of $I_{OFF}$, which is significantly smaller than the MOSFET $I_{OFF}$. The simulation of this TFET has been done using Silvaco Atlas [17] The results of this simulation, using the non-local BTBT model as described in figure 4, show the Id-Vgs characteristics where drain to source voltage is 1V.

![Figure 4. Transfer characteristics of SOI PTFET at $L_{G}=100nm$ and $t_{Si}=20nm$](image)

Therefore, outstanding features of this device are very low OFF current, determined by the p-i-n leakage current, and a swing independent of $Kt/q$ which can be optimized to be less than 60mV/decade, very high $I_{ON}/I_{OFF}$ ratios can be achieved; independent of geometrical scaling which shown in figure 5 and figure 6.

![Figure 5. ON current at $V_{DS}$ is 1V and 0.6V of SOI PTFET at $L_{G}=100nm$](image)

![Figure 6. ON current at $V_{DS}$ is 1V and 0.6V of SOI PTFET at $L_{G}=100nm$](image)

To realize a high tunneling current and steep slope, the transmission probability of the source tunneling barrier
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should become close to unity for small change in \( V_G \). For further improvement in the ON current, three approaches can be considered as follows: the use of lower band gap material, lower Equivalent Oxide Thickness (EOT), and a more abrupt source doping profile. First, the lower band gap material increases the band-to-band tunneling generation rate which is an exponential function of the band gap. Thus, the use of SiGe or Ge will increase the ON current. The lower band gap material can be used in the entire active device area or only in the selected region where the band-to-band tunneling occurs. Since the former optional so increases the OFF current dramatically, which leads to lower ON/OFF current ratio, the latter option is more appropriate. Second, the lower EOT contributes to higher ON current by increasing the coupling between the gate voltage and the channel potential.

![Figure 7. Id-VGs characteristics of SOIPTFET at different tOX](image)

Figure 7. shows the \( I_D-V_{GS} \) characteristics of SOI-PTFET at different gate-oxide thickness variation where \( V_{DS} \) is 1V. This result shows the impact of variation in oxide thickness. The tunneling current increases due to an increase in the electric field at source channel interface. Therefore, in order to improve the performance of the device, the electric field should be increased by decreasing the gate oxide thickness.

\( b). \textbf{Subthreshold Swing of TFET} \)

Since the TFET has a different source carrier injection mechanism than the MOSFET, it can achieve sub-60mV/decade Subthreshold Swing (SS). Author Wang et al. [1] reported the feasibility of the TFET for low-power applications. Zhang et. al [18] provided a theoretical analysis that the SS value of TFET can be reduced below 60mV/decade. Bhuwalka et.al [19] showed a vertical Si/Si-Ge TFET with a SS of 44mV/decade through device simulation. The first tunneling device which has an SS less than 60mV/decade was implemented by Appenzeller et. al [20] based on Carbon Nano Tube (CNT) technology. However, in the case of silicon-based TFETs, there has been no experimental result demonstrating sub-60mV/decade SS. Although, the TFET exhibits an extremely low SS value, its ON/OFF current ratio is lower than that of the conventional MOSFETs. The low ON current stems from the difference of carrier injection mechanisms between the TFET and the MOSFET. It is well known that the band-to-band tunneling current becomes less sensitive to the electric field as the potential difference between the channel and the source increases. Thus, beyond the sub-threshold region, it is difficult to achieve large transconductance.

The subthreshold swing is defined by \( SS = \left( \frac{\partial \log I_D}{\partial V_{GS}} \right)^{-1} \) in units of mV/decade, and in the MOSFET, it is independent of \( V_{GS} \) below the threshold voltage. The SS indicates the minimum amount of gate-voltage reduction necessary to lower the subthreshold current by a factor of ten. For the TFET the derivative of the tunneling current expression of (2) with respect to gate-to-source voltage can be obtained the TFET sub threshold swing [3].

\[
S = \log \left[ \frac{1}{V_R} \frac{dV_R}{dV_{GS}} + \frac{e+B}{e^2} \frac{de}{dV_{GS}} \right]^{-1}
\]

(3)

![Figure 8. Subthreshold swing of MOSFET, TFET and Ideal [3]](image)
V. Conclusion

The SOI-PTFET has been simulated in this work. The nonlocal BTBT physical model using for the accuracy of our proposed model verified from 2D Silvaco ATLAS numerical solutions which gives the drain current characteristics as well as ON/OFF ratio. Hence Tunnel FET transistor has attracted a lot of attention for digital devices such as SRAM as well as in analog and RF applications. In Tunnel FET, the dynamic power dissipation will be decreased since the operating voltage is very low.

References