COMPARATIVE POWER ANALYSIS OF CPG AND SSASPL WITH DIFFERENT TECHNOLOGY

Parimita Bai
Department of Electronics and Communication Engg.
Centre for Advance Post Graduate Studies,
Rourkela Biju Patnaik University of Technology,
Odisha, India

Priteesa Mahapatra
Department of Electronics and Communication Engg.
Centre for Advance Post Graduate Studies,
Rourkela Biju Patnaik University of Technology,
Odisha, India

Abstract:
This paper describes a comparative analysis of proposed low power shift resister using SSASPL (Static differential sense amplifier based shared pulsed latches) and pass logic based 4 bit CPG (clock pulse generator). The pass logic based CPG has been designed which generate small clock pulse with small pulse width. These pulses are given to the proposed shift resister for high speed. The system is designed using cadence virtuoso 180nm technology and cadence virtuoso 45nm technology. The maximum supply voltage is 1.8V. The proposed design using cadence virtuoso 45nm technology reduces the power by.

Keywords: low power, latches, SSASPL, clock pulse generator, 180nm, 45nm.

I. INTRODUCTION:
Low power circuit has emerged as a main theme in today’s electronic industry. While area, speed, cost are also other important parameter to be consider. Shift resister is important building block of digital design. Shift resister are used in many application such as digital filter[2], communication receiver[3] and image processing [4] and audio decoder circuit in multimedia processor, data conversion between parallel to serial or serial to parallel, counter, parity generator. Shift resister are the combination of many flip-flop with separated clock signal. This type of flip-flop operate in high frequency but generally consume high power due to more number of transistor and large clock load. Flip-flop can be replaced with pulsed latches to design a low power shift resister but the latch cannot be connected serially like flip flop due to the timing problem. The timing problem can be solved using delay circuit.

The delay circuit can be used in between the latches or in between the clock pulse for designing shift resister. The addition of delay circuit also increases the power consumption. [2]

The conventional shift resister has designed using SSASPL and 4-bit clock pulse generator. SSASPL contain less no of transistor hence consume low power. [1] The SSASPL in fig-1 updates the data with three NMOS transistor and hold the data with four transistors in two cross coupled inverter.

Fig.1. (Schematic of SSASPL)
The delay pulse is provided to the SSASPL which is generated by clock pulse generator. A clock pulse generator is a combination of serially connected single pulse generating circuit. [2][4] Each single clock generating circuit contains one CMOS AND gate, buffer and delay circuit as in fig-2.

Fig.2 (Single Pulse Clock Generator)

Single clock pulse generating circuit. A 4bit CPG is the combination of five single clock pulse generating circuit. Which generate five delayed clock pulse?

The CPG is used to design 16bit shift resistor. The 16bit shift resistor divided into 4 sub shift resistor of 4bit. Each sub shift resistor contains 5 latches. The four latches used to transfer the data and fifth latch is used to store the data temporarily. Total no of twenty latches can be used to store and transfer the data in a 16bit shift resistors. [3][4]

Fig.3. (Pulsed Clock Generator)

II. PROPOSED DESIGN:

1. The proposed single clock pulse generator consist of 14 transistor designed in cadence virtuoso 45nm technology. [2] as like in fig-4

Fig.4. (Conventional single clock pulse Generator)

2. The modified CPG is designed by connecting five pass logic based single clock pulse generating circuit. Which generate five delay clock pulse with reduced width? The modified CPG consist of 70 transistors. [1]

Fig.5. (Modified single clock pulse generator)
3. The generated 5 clock pulse can be given to the shift register for low power consumption as like fig7

**III. RESULTS**

Transient response

The wave form here are given for the propose SSASPL latch and modified CPG

Fig-8 shows the transient response of SSASPL in which clock pulse period consist of 10ns and input d consist of 10ns.

**Fig.9. (Waveform of single clock pulse generator)**

Fig-9 represents the waveform of modified single clock pulse generator in which a reduced Clock pulse width has been generated.

**Fig.10. (Waveform of modified CPG)**

Fig-10 represents the wave form of modified CPG In which a series of delayed clock pulse with reduced width is generated. The clock signal is consist of 10ns period
### III. PERFORMANCE COMPARISON

**TABLE 1**

Comparison of avg. power consumption of SSASPL

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Technology</th>
<th>180nm</th>
<th>45nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 MHz</td>
<td>63.35μW</td>
<td>21.93μW</td>
<td></td>
</tr>
<tr>
<td>100 MHz</td>
<td>7.282μW</td>
<td>2.193μW</td>
<td></td>
</tr>
<tr>
<td>500 MHz</td>
<td>3.664μW</td>
<td>2.186μW</td>
<td></td>
</tr>
</tbody>
</table>

**TABLE 2**

Comparison of avg. power consumption of single clock pulse generator

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Technology</th>
<th>180nm</th>
<th>45nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>184.7μW</td>
<td>17.28μW</td>
<td></td>
</tr>
<tr>
<td>100</td>
<td>18.46μW</td>
<td>10.731μW</td>
<td></td>
</tr>
<tr>
<td>500</td>
<td>4.387μW</td>
<td>348.6nW</td>
<td></td>
</tr>
</tbody>
</table>

**TABLE 3**

Comparison of avg. power consumption of clock pulse generator

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Technology</th>
<th>180nm</th>
<th>45nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 MHz</td>
<td>720μW</td>
<td>102.7μW</td>
<td></td>
</tr>
<tr>
<td>100 MHz</td>
<td>83.47μW</td>
<td>10.28μW</td>
<td></td>
</tr>
<tr>
<td>500 MHz</td>
<td>16.68μW</td>
<td>2.063μW</td>
<td></td>
</tr>
</tbody>
</table>

### IV. CONCLUSION

A low power CPG and SSASPL has been designed using cadence virtuoso 45nm technology. 45nm is the minimum possible channel length of the transistor. A 4-bit clock pulse generator, single clock pulse generating circuit and SSASPL latch has been designed with maximum supply $v_{dd}=1.8v$ where the proposed clock pulse generator save 14% average power consumption and single clock pulse generating circuit saves 34% power consumption.

### V. REFERENCES

1. IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 62, NO. 6, JUNE 2015Low-Power and Area-Efficient Shift Register Using Pulsed Latches Byung -Do Yang
2. IJECT Vol. 7, Issue 2, April - June 2016 ISSN : 2230-7109 (Online) | ISSN : 2230-9543 (Print) 30 International al Journal of Electronics & Communication Technology www. Iject . Org Comparative Analysis of Pulsed Latch and Flip-Flop based Shift Registers for High-Performance And Low-Power Systems 1P. Rajesh, 2D. Suresh Chandra, 3L. Sai Kumar, 4G. Kaushik 1,2,3,4Dept. of ECE, Raghu Engineering College, Visakhapatnam, India
4. THE CMOS INVERTER, chap-5, sep.1999, bwrcs.eecs.berkeley.edu/Classes/icdesign/ee141_f01/Notes/chapter5.pdf